Strategic EHS Considerations in Selection of Next Generation Fab Materials

ERC Retreat & IAB Meeting

Jim Harrison

August 21, 2003

Agenda

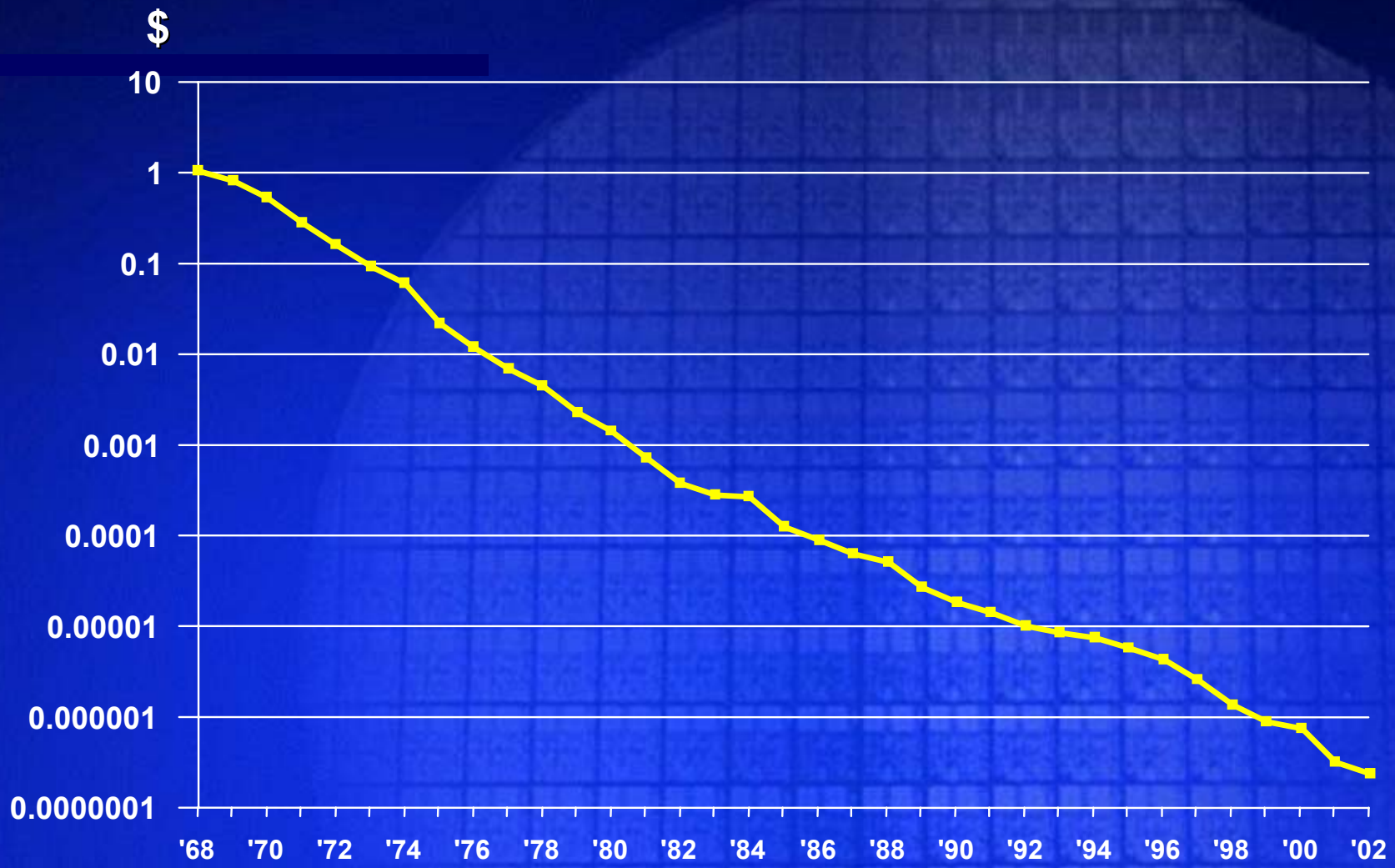
- Business Driver: Moore's Law
- Technical Challenges
- EHS Technical Challenges
- Other EHS Challenges
- Intel Approach
- SRC Opportunities

Business Driven by Moore's Law

Worldwide Semiconductor Revenues

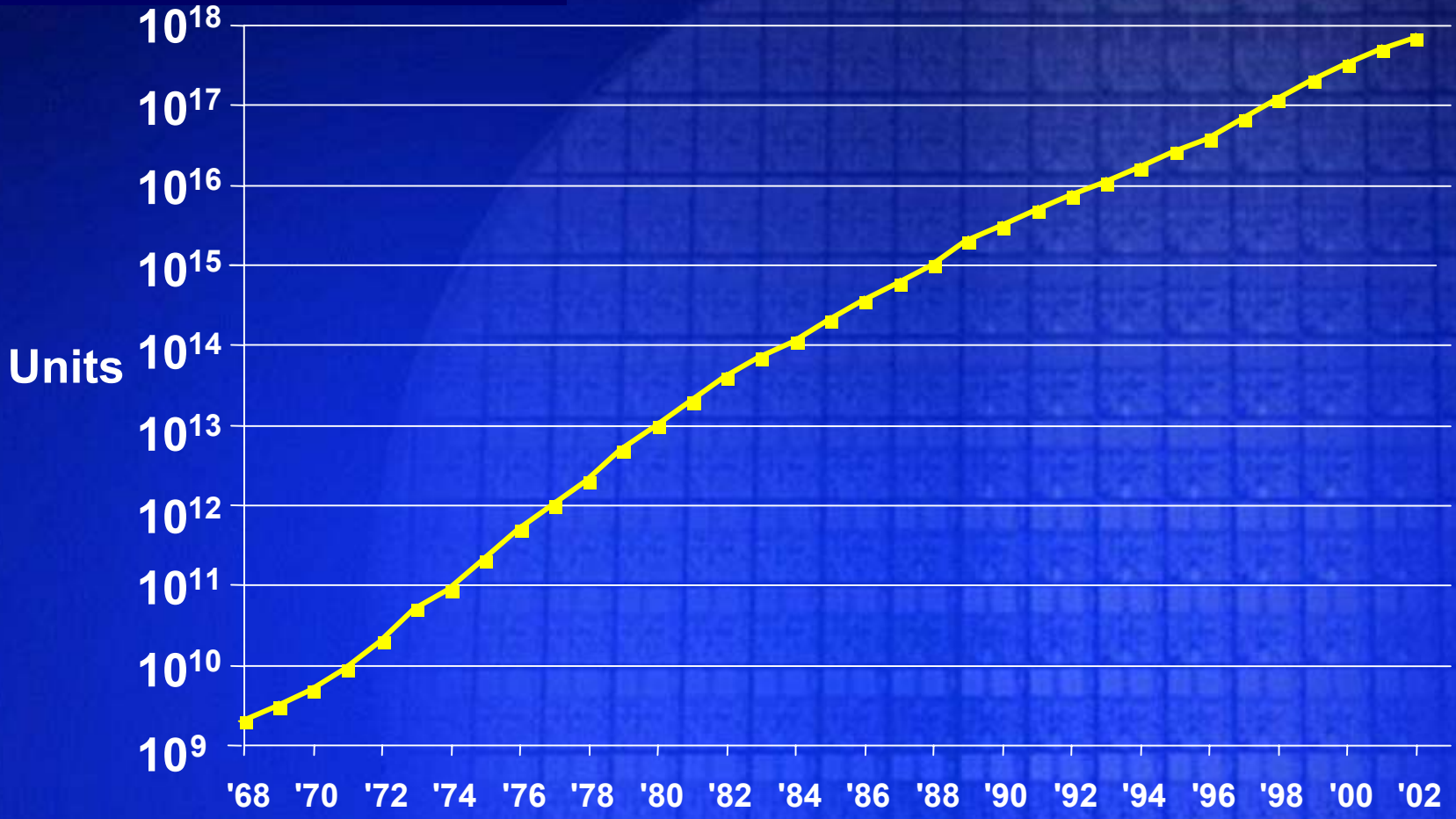
Source: Intel/WSTS,12/02

Average Transistor Price By Year



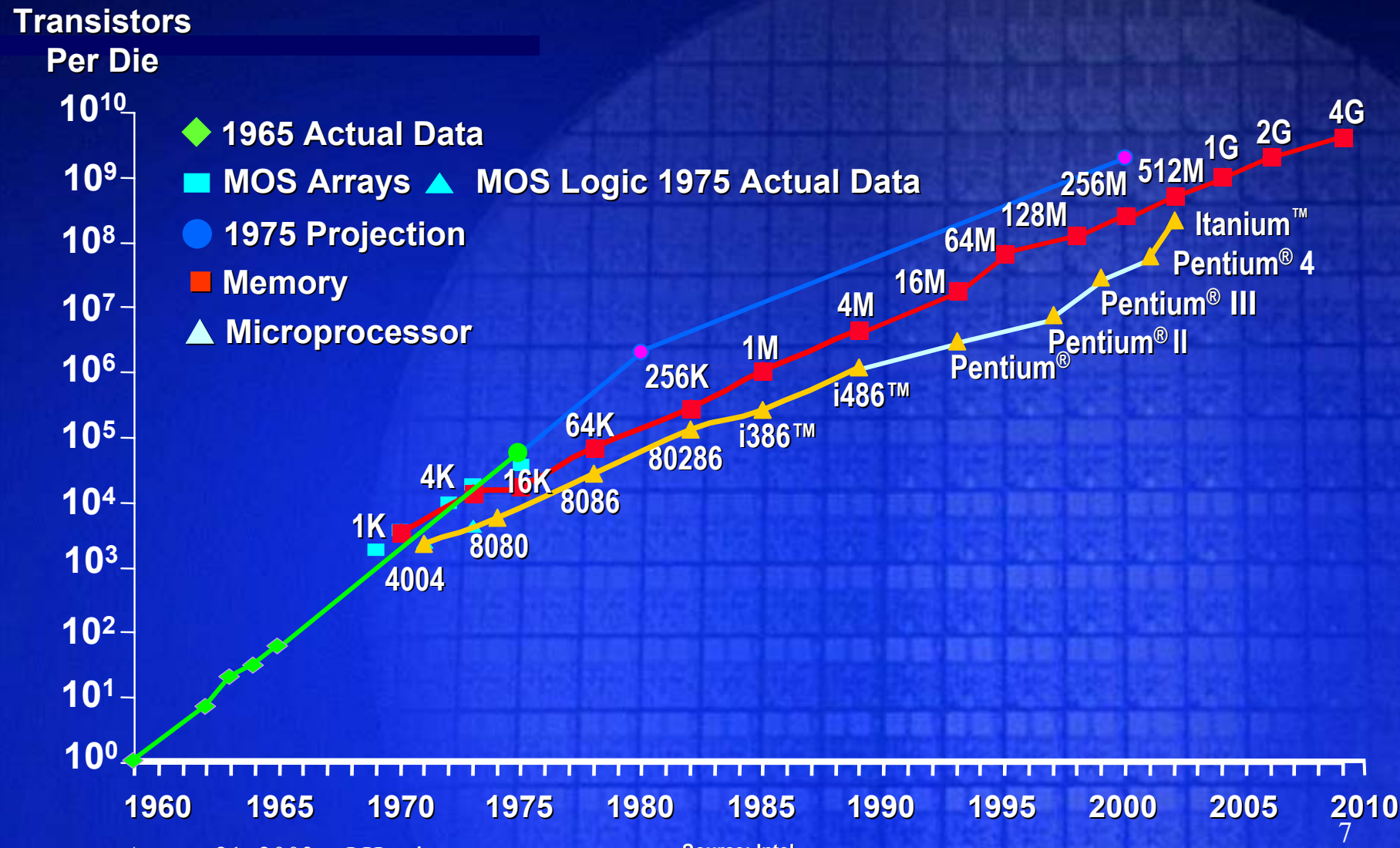
Source: Dataquest/Intel12/02

Transistors Shipped Per Year



Source: Dataquest/Intel, 12/02

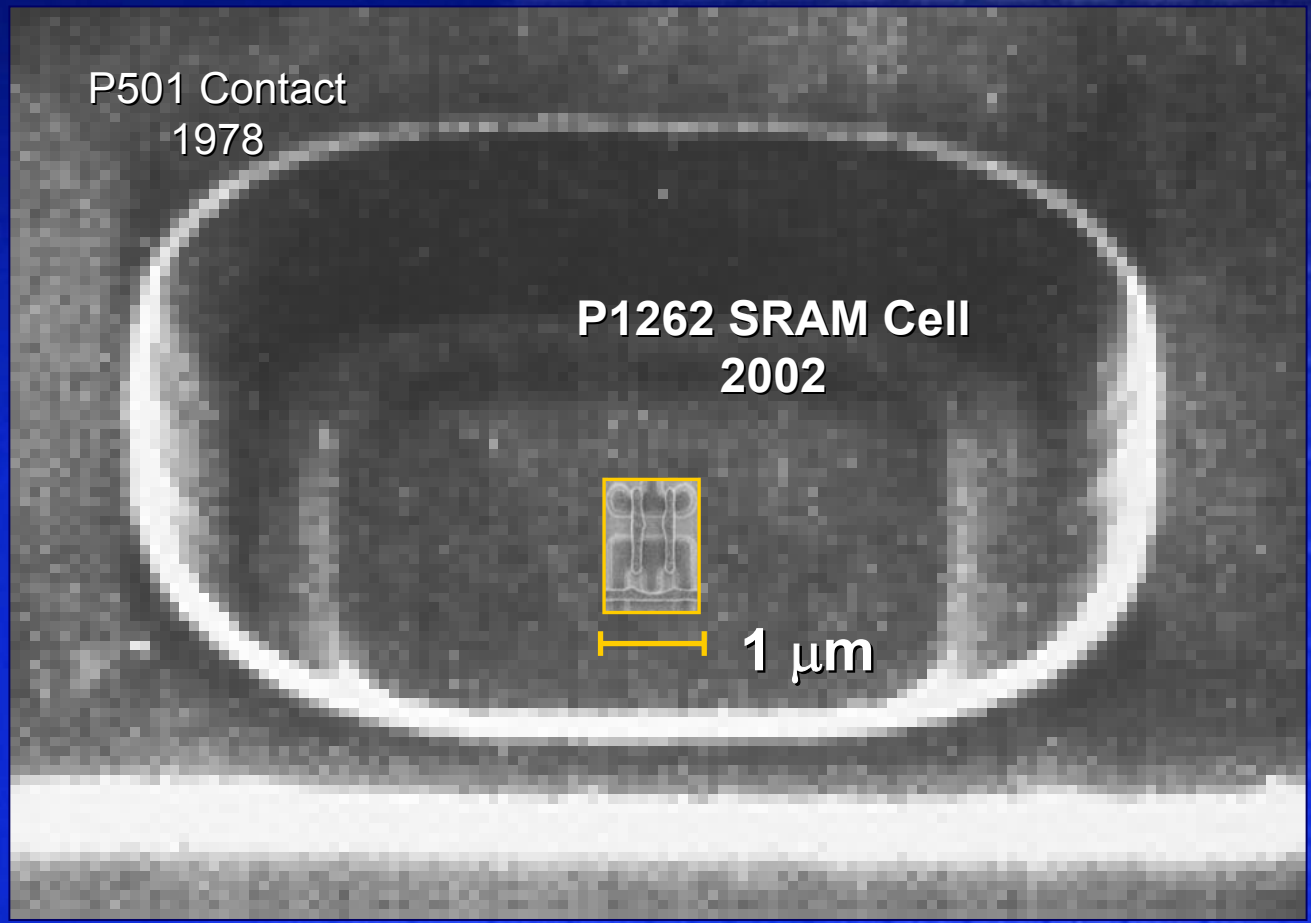
Integrated Circuit Complexity



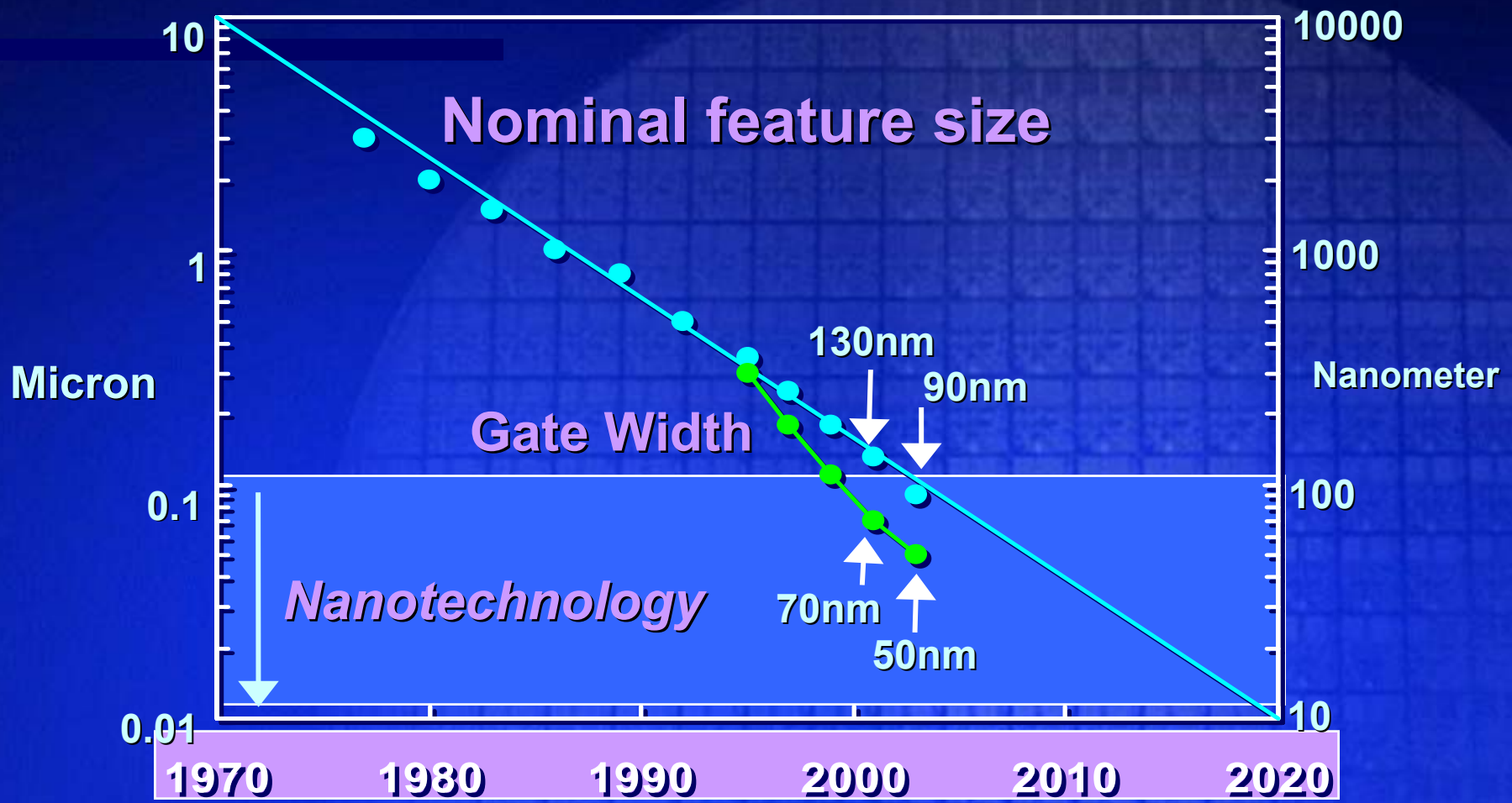
Source: Intel

Technical Challenges of Moore's Law

1 μm² SRAM Cell

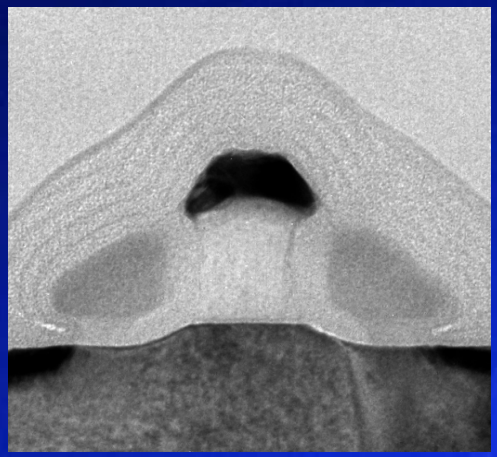


Age of Nanotechnology

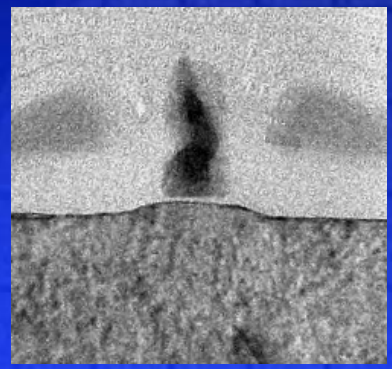


Intel's Transistor research down to 10nm

Experimental transistors for future process generations

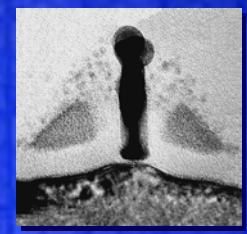


65nm process
2005 production



45nm process
2007 production

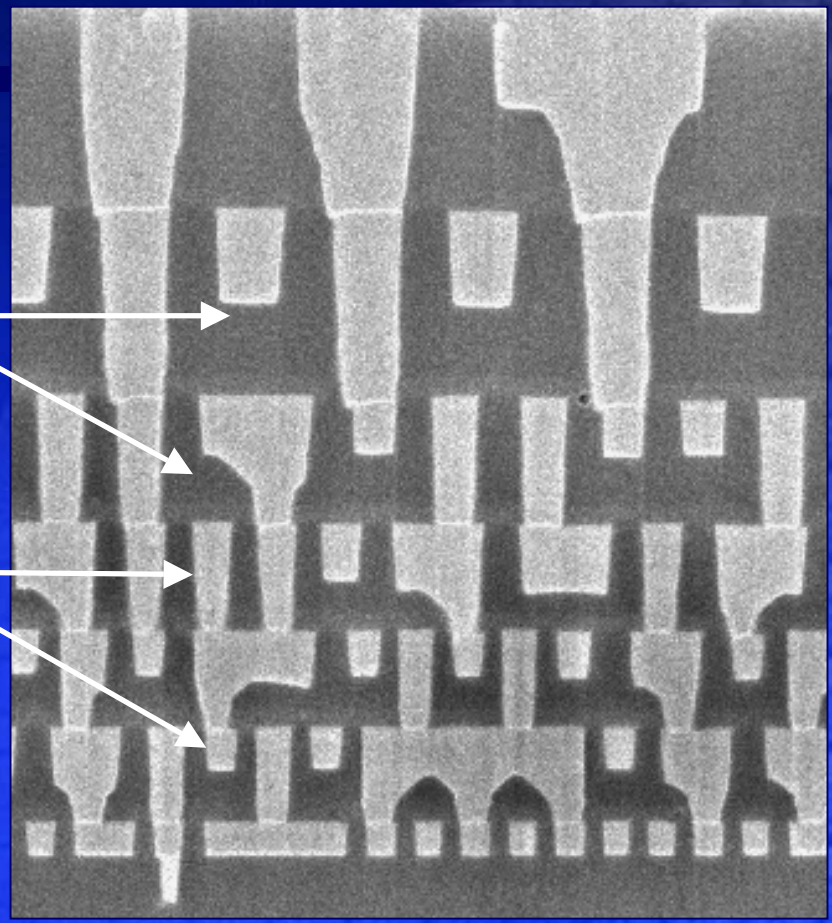
32nm process
2009 production



22nm process
2011 production

We are investigating several options at <10nm

90 nm Generation Interconnects



Low-k CDO Dielectric

Copper Interconnects

Combination of copper + low-k dielectric now meeting performance and manufacturing goals

New Materials and Device Structures Extending Transistor Scaling

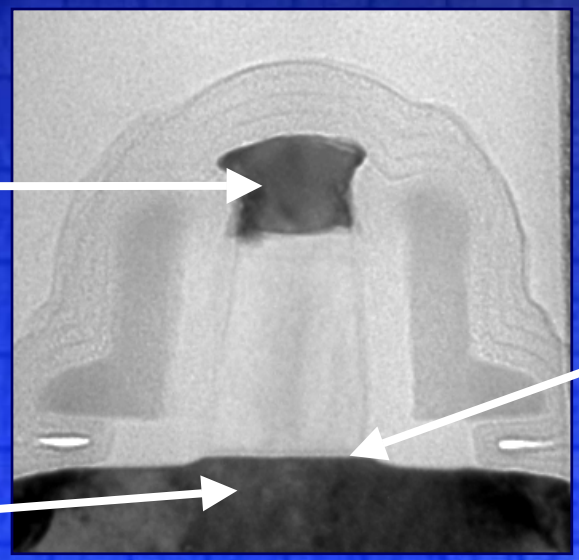
Changes Made

Gate

Silicide Added

Channel

Strained Silicon



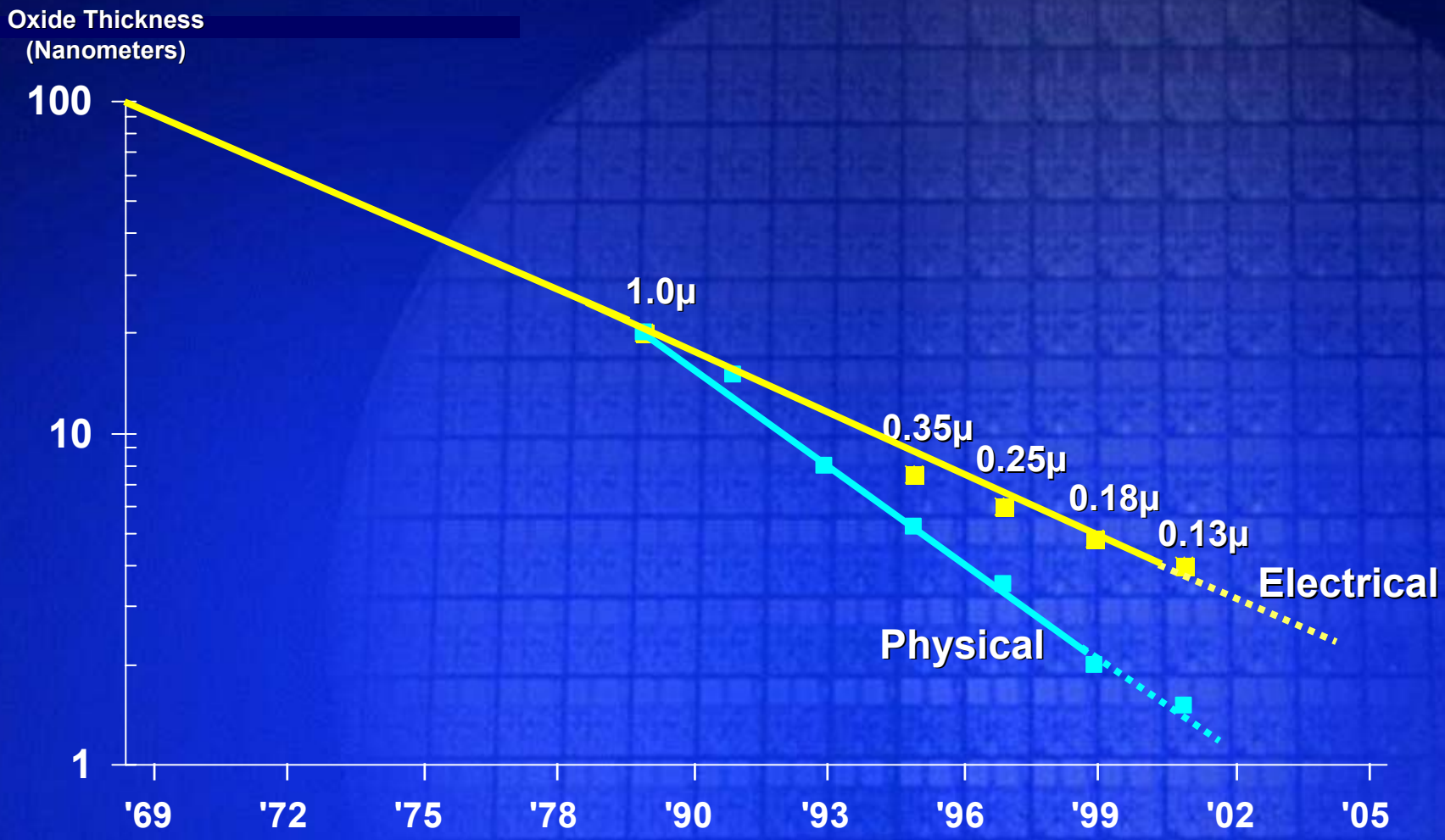
Transistor

Future Options

High-k Gate Dielectric

New Transistor Structure

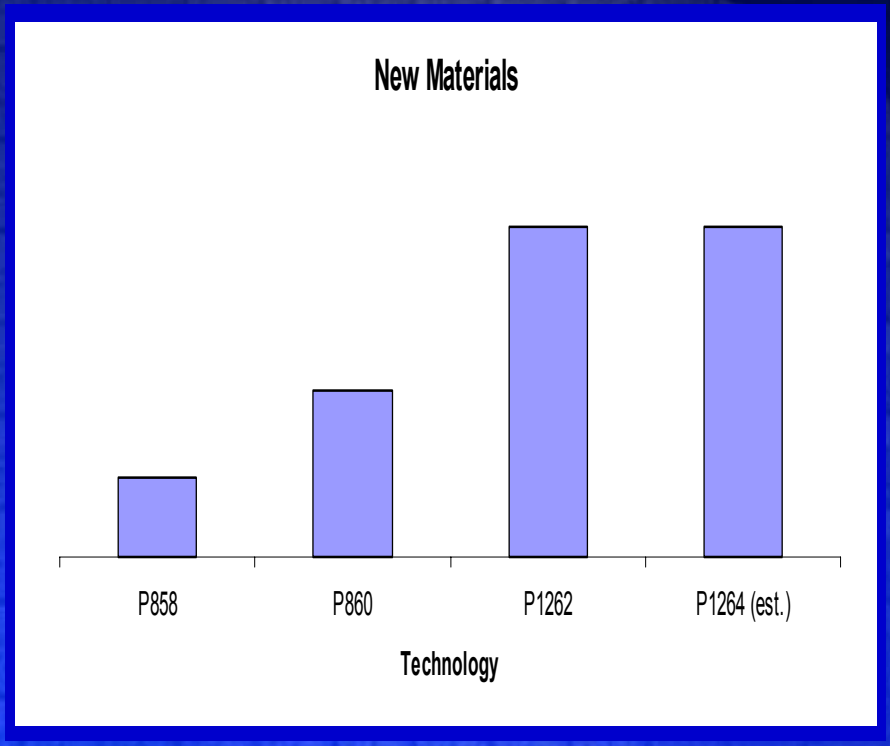
Minimum Insulator Thickness vs Time



Source: Intel

Nanotechnology Environmental Challenge Drivers – Increases in:

- Manufacturing "Si" Area
- Total # of Materials
- New & Novel Materials
- Industry & Company Unique Materials
- Supply Chain Globalization
- Pre-cursors
- Transistor Architecture Options



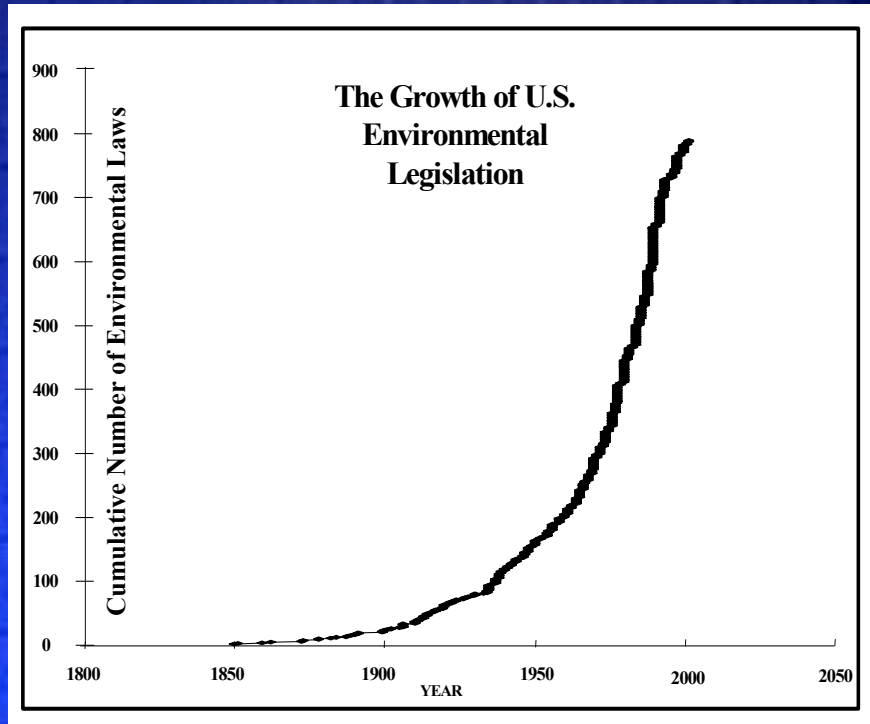
Specialty materials evaluated

–2001 hundreds of materials

–2003 thousands of materials

Other Environmental Challenge Drivers:

- Regulation Globalization
  - "Superset approach"
  - Competitive
- Product ecology
- Manufacturing process Environmental performance a "competitive issue"
- Community Citizenship
- Recent Concerns
  - PFOS
  - REACH
  - Chemical Hazard properties



The EU Legislative Environment

- Intel takes the European regulatory environment very seriously.
- The EU's legislating of Products has an automatic impact on not only Intel's largest investment in Europe, our Fabs in Ireland (around € 5 billion by 2005) but also on our worldwide operations because of Intel's '*Copy Exactly*' methodology for manufacturing
- Intel is preparing our programs to satisfy WEEE and RoHS.
- Future legislation on the eco-design of products and energy efficiency (EUP) and other areas are in discussion with no data on WEEE and RoHS performance.
- Regulatory actions can be burdensome, sometimes overlap and potentially disproportionate to the environmental problems they are trying to solve
- Intel is working with EU regulators and stakeholders to ensure a coherent approach to future environmental policy-making based on sound science and true environmental improvements

Intel's Guiding Principles

Principles

- Prevent all injuries in the workplace
- Be an ESH leader in our communities and our industry
- Reduce the environmental footprint of our products, processes and operations

Rationale

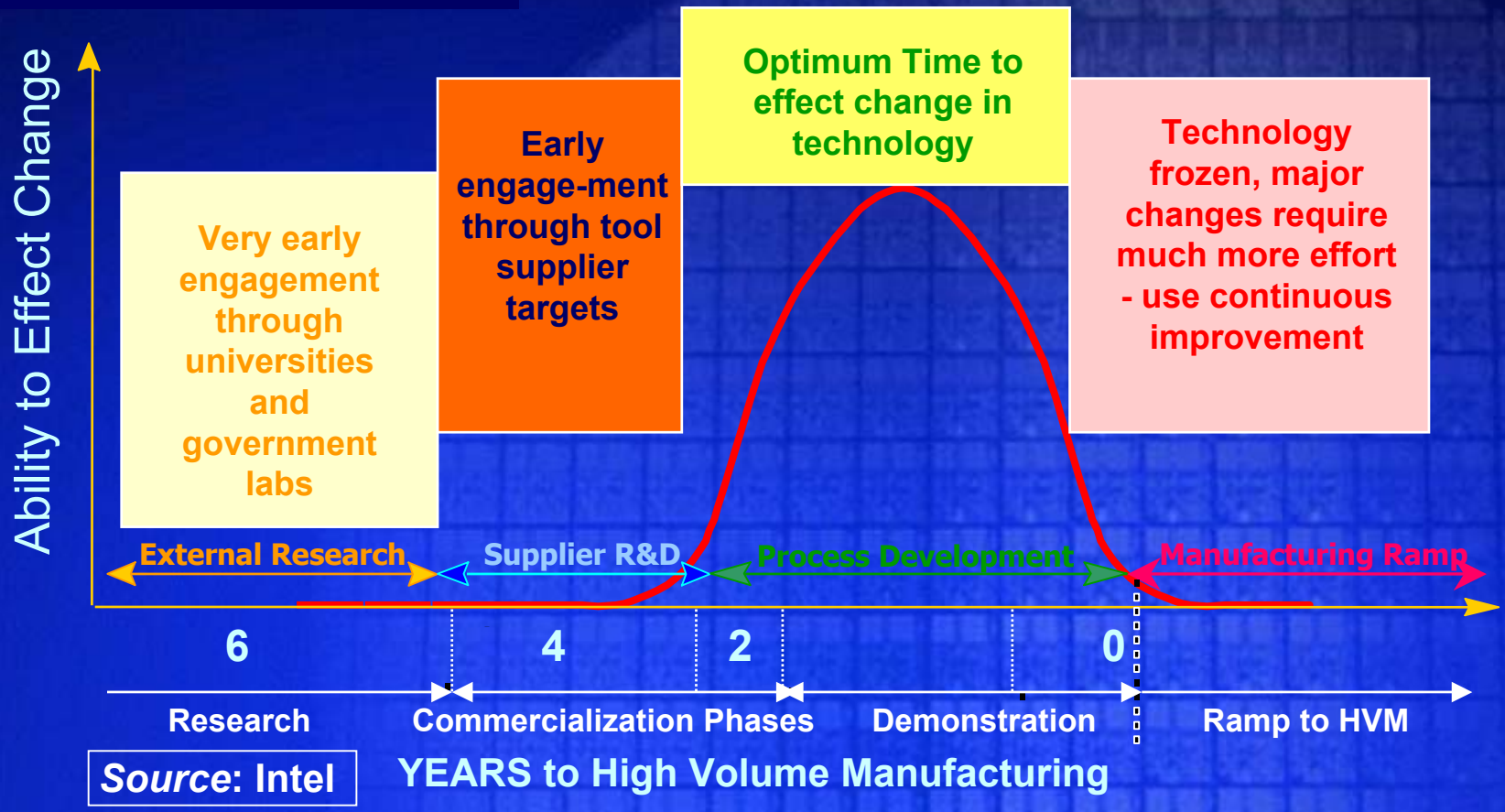
- It's the Right Thing to do!
- Triple Bottom Line:
  - Financial Performance – Return on Investment
  - Social and Community Commitments
  - The Environment – Natural Resource Sustainability
- Part of Intel's Values
- Operational Excellence

What We Do

- Support & Role Model EHS at the Top
- Clear EHS Policy
- EHS Goals owned by the Operations
- Measure and Report EHS Performance
- Extend EHS to Supply Chain
- "Safety First" & Live It!
- Treat the Community as a Customer

- EHS Policy Signed by Craig Barrett, CEO
- Quarterly EHS Operations Review
- Design for EHS integrated with Technology Development
- Employee surveys demonstrate strong support by management for EHS

EHS Technology Engagement Model



Source: Intel

Rapid Technology Changes

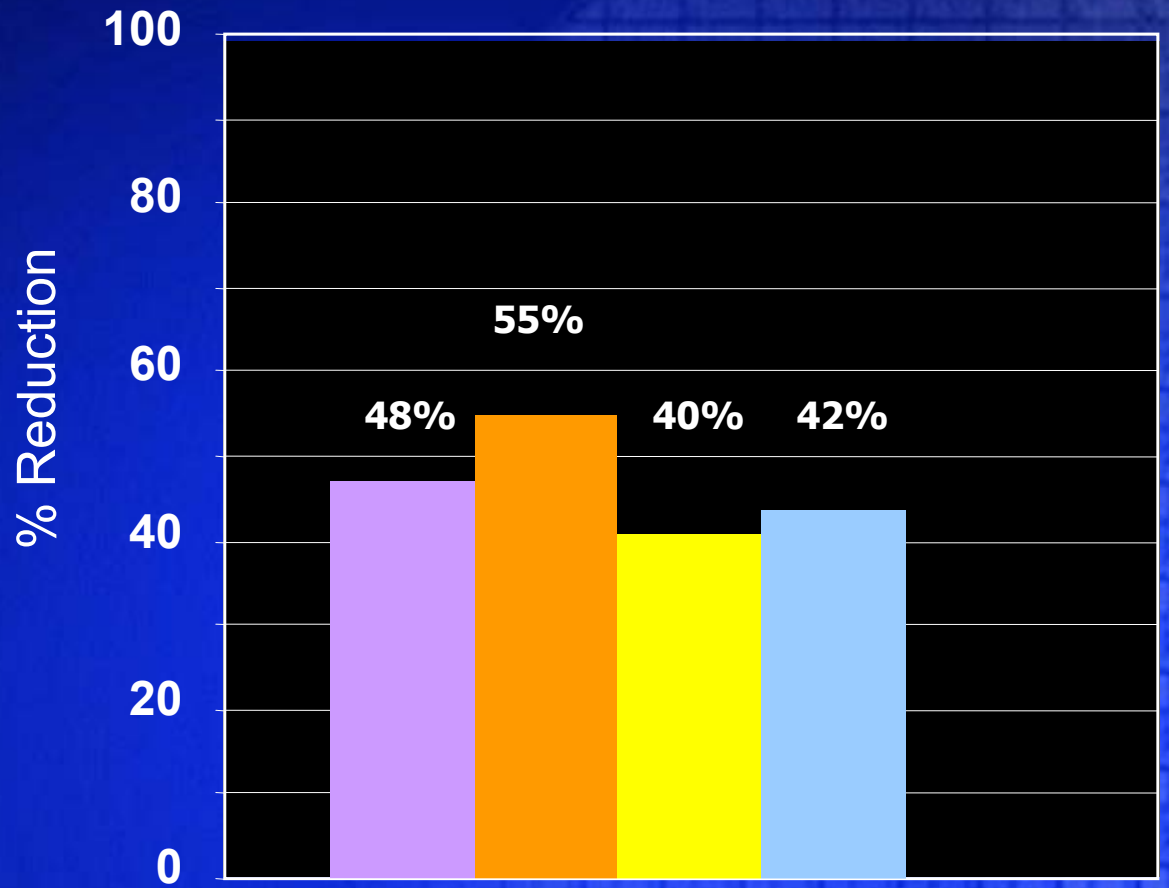
- **New manufacturing process every 2 years:**
  - Parallel efforts - 30 month development cycles
  - Upfront ESH Goals for each technology
  - Cross organizational team own ESH goals and ESH roadmap
  - ESH Goals comprehend "Virtual Factory"
  - Generational Environmental Footprint flat or shrinks
- **Intel "Copy Exactly" transfer methodology**
  - Rapid Ramps
  - Consistent predictable performance

DFESH

- **ESH integrated throughout the TD process:**
  - Chemical Use Policy and Approval Process
  - Manufacturing Process development
  - Chemical & Equipment selection
  - Waste Management
  - Facility design
  - Ergonomics and Equipment Safety
  - Manufacturing equipment selection
- **Materials go through Material and Supply Chain Risk Assessment & Mitigation process**
- **Piloting programs with Suppliers around Chemical Data**

Estimated 300mm Emissions & Water Use Relative to 200mm

300mm is more Environmentally Friendly



- Volatile Organic Compounds
- Perfluorocarbons
- Hazardous Air Pollutants
- Ultra-pure water

Vendor supplied data

Source: Intel

Environmental Performance 2002

Intel's EHS Report: www.intel.com/go/ehs

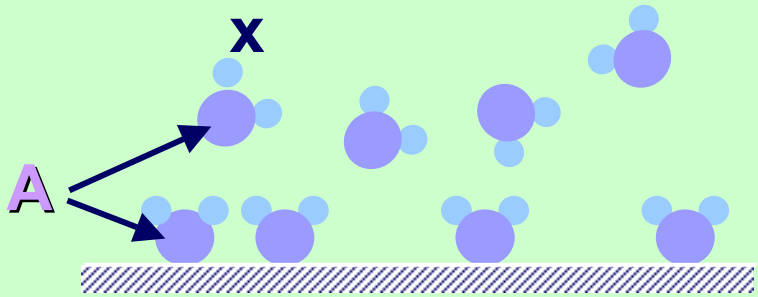
- >55% of Chemical Waste recycled worldwide
- >65% of Solid Waste recycled worldwide
- Fresh water usage 16 million gal./day worldwide
- 30% reduction in VOC emissions since '99 (218 tons worldwide)
- Global warming emissions 1.03 MMTCE (includes electricity usage)
- 30,000 PCs refurbished and delivered to schools and non-profit organizations

ERC for EBSM support

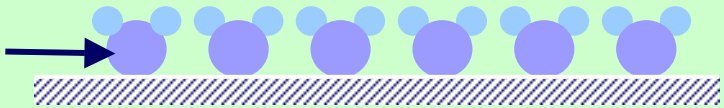
- Maintain scientific integrity of program
- Source of future Industry scientists & leaders
- Characterization method's and model's
- Safe use practices & Lifecycle understanding
- Identify lower ESH footprint alternatives
  - Examples: PFOS, PFC, Pb, Slurries, Resist strippers etc

Backup

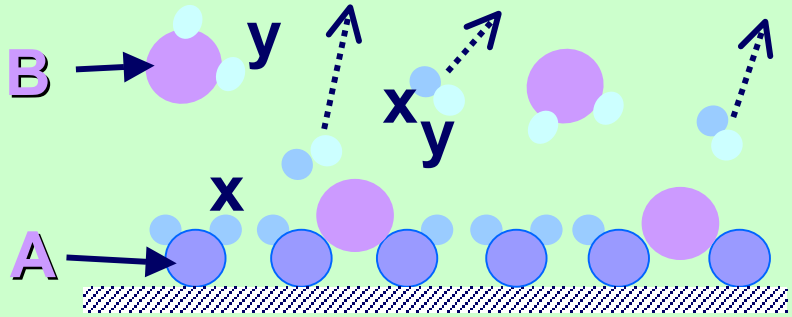
Crafting Films with Atomic Layer Deposition



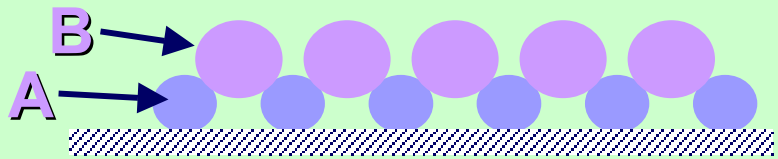
Step 1



Step 2



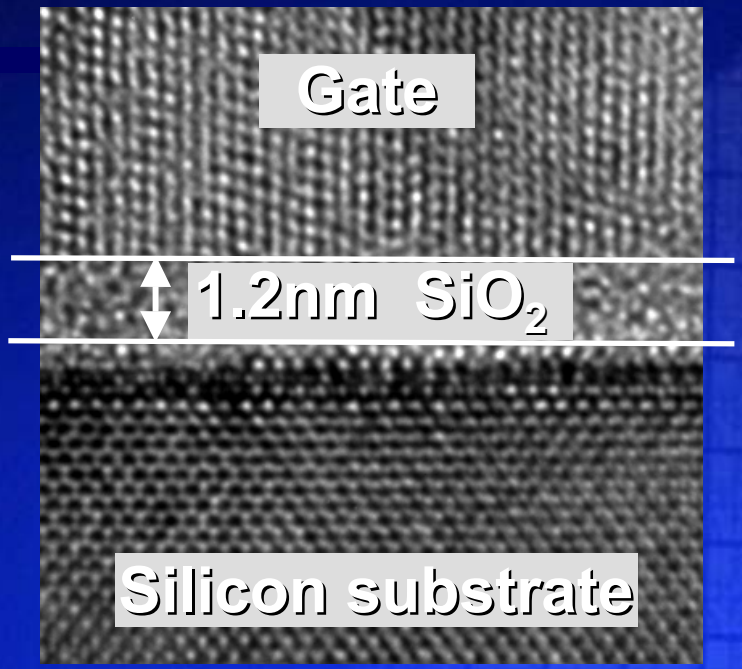
Step 3

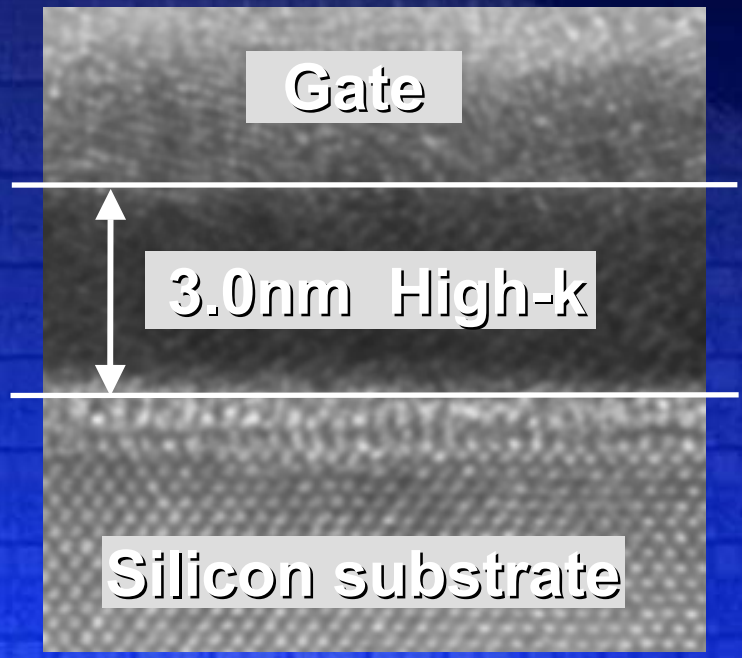


Step 4

ALD: Today's nanotechnology for self-assembly by atomic layer

High K for Gate Dielectrics





90nm process

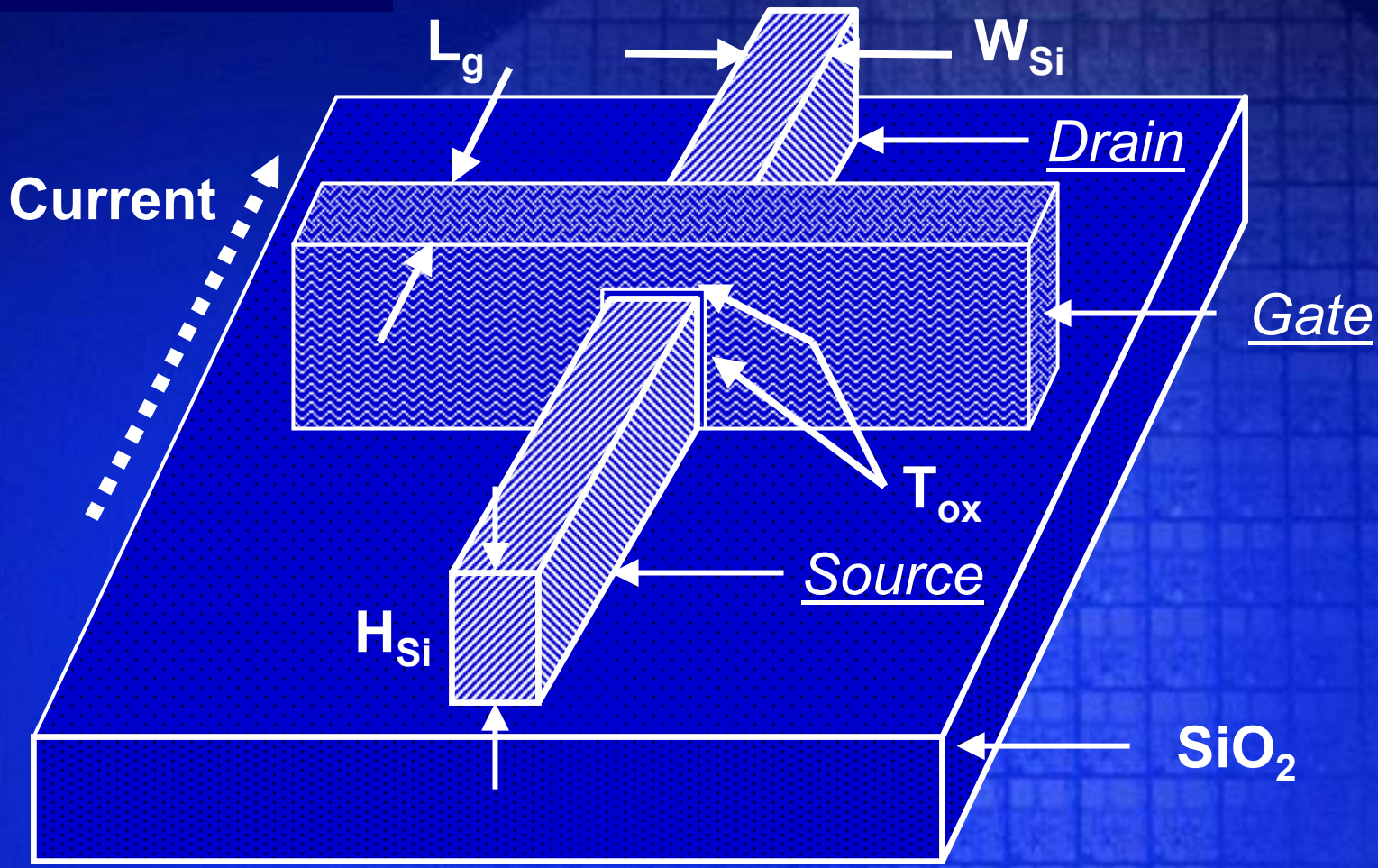
Capacitance	**1X**
Leakage	**1X**

Experimental high-k

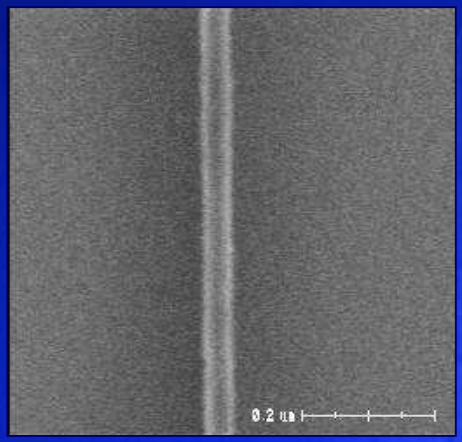
1.6X
< 0.01X

Source: Intel

Tri-Gate Transistor Structure

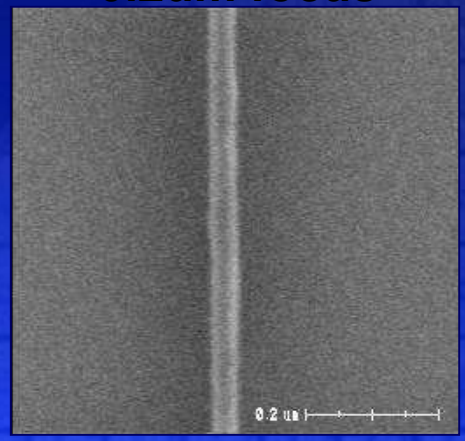


50nm Resist Lines With 193nm Light

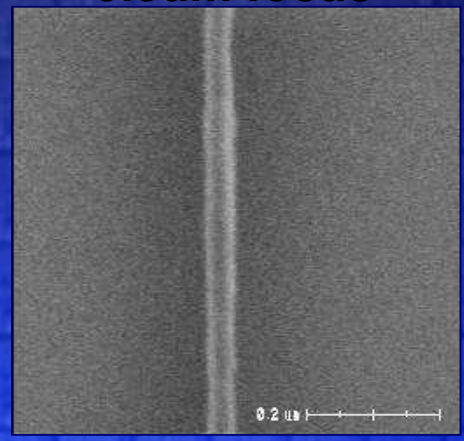


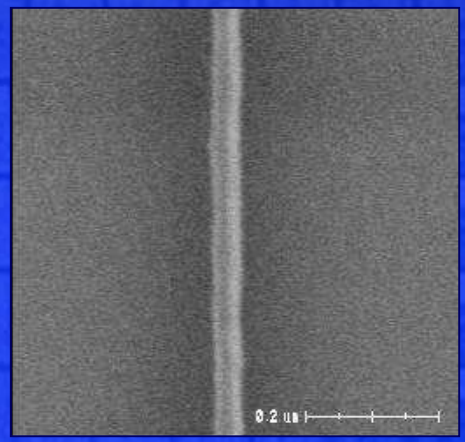
"best focus"

-0.2um focus

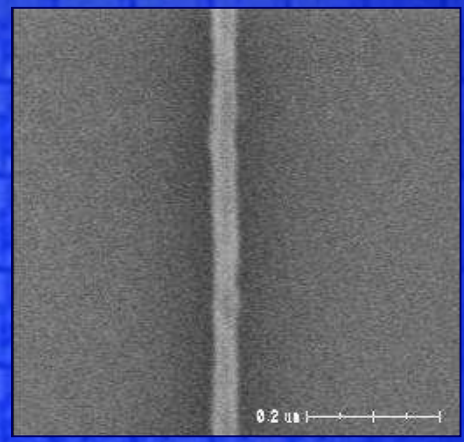


-0.3um focus





+0.2um focus



+0.3um focus